Zachary Chen (650) 861-8685 | zacharyzgc@gmail.com

Education

Purdue University: Bachelor of Science in Electrical Engineering

Concentration: Microelectronics and Semiconductors

Relevant Coursework:

Computer Design and Prototyping, ASIC Design Lab, Microprocessor Systems and Interfacing, Advanced C Programming, Digital System Designs, Digital Systems Senior Project

Projects

Dual-Core Pipelined MIPS Processor

- Designed and implemented dual-core pipelined processors with forwarding unit, hazard unit, 2-way set associative write-back dcache, icache, bus controller for arbitration and to maintain cache coherence(MSI).
- Achieved >50 MHz max clock speed when synthesized and running mergesort.asm(LAT=10) on FPGA and analyzed speedup compared to previously implemented single cycle and cache-less designs.
- Verified functionality and performance of modules by writing testbenches, simulating and analyzing waveforms on QuestaSim, synthesizing onto Altera DE2 FPGA, writing and running assembly unit tests on processor design.

USB Full-Speed Bulk-Transfer Endpoint AHB-Lite SoC Module

- Designed and implemented USB endpoint support module to an AHB-Lite based SOC.
- Implemented RX module with bit stuffing detector, Sync byte detection, PID identification, EOP detector, NRZ decoder, CRC checkers.
- Managed Git repository to centralize module files between team members to integrate the RX, TX, and AHBlite modules in the top-level file.

AHB-Lite FIR Filter Accelerator Design and Verification

- Designed and implemented AHB-lite slave with 4-point High-Pass convolutional FIR filter to create FIR filter module in SystemVerilog used for edge detection on an image.
- Verified design by developing test benches and analyzing QuestaSim waveforms for top-level module, AHBlite module, and FIR Filter module.

Work Experience

AI and Machine Learning Co-op | Stellantis

- Created battery depletion calculator in Python that will be used for optimizing drive mode switches within the ADAS coaching feature in plug in hybrid electric vehicles.
- Researched, documented, and presented models of Destination Prediction using Markov Chain to integrate AI tools to the driver cockpit.

Motor Controls Co-op | Stellantis

- Developed MATLAB Simulink model of a software component from C code to allow for better modeling and simulation of software-in-the loop vehicles.
- Created test harness using Simulink and ran simulation to validate the performance of the model.

EE Validation Co-op | Stellantis

- Root caused issues on hardware-in-the-loop vehicles and plywood buck by analyzing oscilloscope waveforms and simulating signals to device under test.
- Developed, documented, and executed test procedures for four vehicle functions in a streamlined and effective manner, ensuring quality and functionality of tested functions.

Technical Skills

Programming	ASIC	Computer	Other
Languages:	Design:	Architecture	Skills:
C/C++	SystemVerilog	5-stage pipeline	MATLAB Simulink
Python	QuestaSim	Cache Design/Coherence	Git Version Control
MATLAB	Vivado	Hazards / Exceptions	Arduino IDE
Java	Synopsis Design Compiler	Virtual Memory /TLB	KiCad / PCB design
RISC-V / MIPS	UVM	Basic GPU Architecture	Embedded System Design

December 2023

October 2023

May 2023 – August 2023

May 2022 – August 2022

August 2021 – December 2021

May 2024

April 2024